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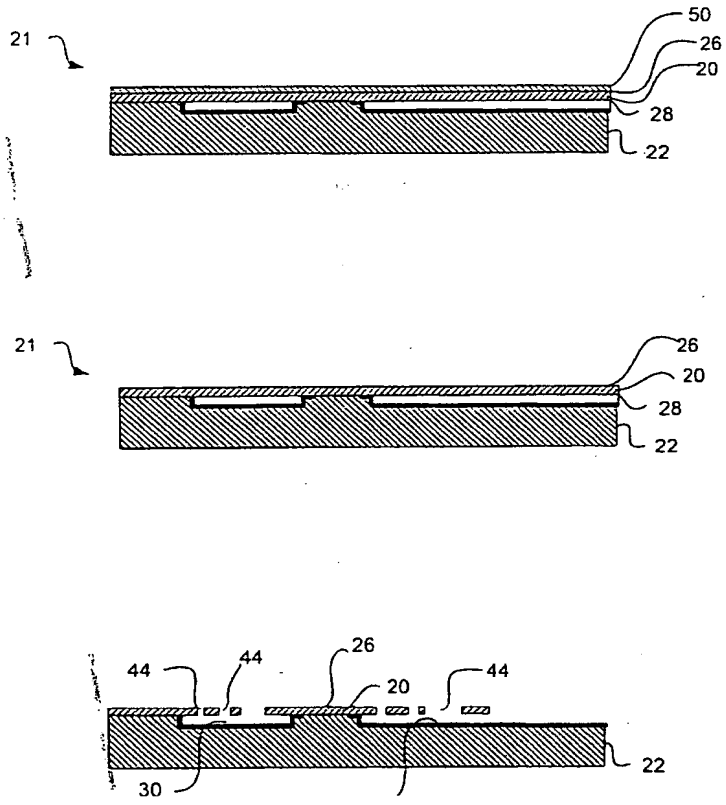

(57) Abstract: Methods for making thin silicon layers suspended over recesses (30) in glass wafers (22). One method includes providing a thin silicon-on-insulator (SOI) wafer (21), and a glass wafer (22). The SOI wafer (21) can include a silicon oxide layer (50) disposed between a first undoped or substantially undoped silicon layer (20) and a second silicon layer (60). Recesses (30) can be formed in the glass wafer surface (24) and electrodes (38) may be formed on the glass wafer surface (24). The first silicon layer (20) of the SOI wafer (21) is then bonded to the glass wafer surface (24) having the recesses (30), and the second silicon layer (60) is subsequently removed using the silicon oxide layer (50) as an etch stop. Next, the silicon oxide layer (50) is removed. The first silicon layer (20) can then be etched to form the desired structure. In another illustrative embodiment, the first silicon layer (120) has a patterned metal layer (129) positioned adjacent the recesses (30) in the glass wafer (22). The, the second silicon layer (60) is removed using the silicon oxide layer (50) as an etch stop, and the silicon oxide layer (50) is subsequently removed. The first silicon layer (120) is then etched using the patterned metal layer (129) as an etch stop. The patterned metal layer (120) is then removed.

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SOI/GLASS PROCESS FOR FORMING THIN SILICON MICROMACHINED STRUCTURES

Cross-Reference to Co-pending Patent Applications

This application is related to co-pending U.S. Patent Application Serial No. _____ [1100.1116101], entitled "THIN SILICON MICROMACHINED STRUCTURES", filed on date even herewith and incorporated herein by reference.

Field of the Invention

The present invention is related generally to semiconductor manufacturing and Micro Electro Mechanical Systems (MEMS). More specifically, the invention relates to methods for providing thin silicon micromachined structures.

Background of the Invention

Micro Electro Mechanical Systems (MEMS) often utilize micromachined structures such as beams, slabs, combs, and fingers. These structures can exhibit curvature due to internal stresses and doping gradients. The curvature can be a significant source of error in inertial sensors such as accelerometers, tuning forks, and gyroscopes. Many desired structures have a flatness design criteria that is difficult or impossible to achieve using current processes. In particular, silicon layers heavily doped with boron can have a significant curvature when used in suspended structures.

The aforementioned structures are often made starting with a silicon wafer substrate. A boron-doped silicon epitaxial layer is then grown on the silicon wafer substrate and is subsequently patterned in the desired shape. As is further described below, the boron is used as an etch stop in later processing to allow for easy removal of the silicon substrate, leaving only the thin boron-doped epitaxial layer.

At the interface between the boron-doped epitaxial layer and the silicon substrate, the boron tends to diffuse out of the epitaxial layer and into the silicon substrate. This depletes the epitaxial layer of some boron, and enriches the silicon substrate with boron. The epitaxial layer thus often has a reduced concentration of boron near the interface, which is sometimes called the "boron tail."

After the boron-doped silicon epitaxial layer has been grown to the desired thickness, the silicon substrate is often removed using an etchant that is boron selective. Specifically, the etchant will etch away the silicon substrate, but not the

boron-doped silicon epitaxial layer. One such etchant is a solution of ethylene diamine, pyrocatechol, and water (EDP). The etchant typically etches the silicon at a fast rate up to a certain high level boron concentration, at which point the etch rate significantly slows. This high boron concentration level is termed the etch stop level.

The boron concentration near the epitaxial layer surface having the boron tail may be lower than the etch stop level, allowing the etching to remove some of the epitaxial layer surface at a reasonable rate, stopping at the etch stop level of boron concentration beneath the initial surface. The resulting boron-doped structure, such as a beam, thus has two surfaces, the silicon side surface that has the boron tail and the airside surface that has a boron surface layer concentration substantially equal to the concentration in the bulk of the beam away from either surface. Thus, the opposing surfaces have different boron surface layer concentrations.

The building of a suspended element often includes using an epitaxially grown single-crystal silicon heavily doped with boron, for example, greater than ten to the twentieth atoms per cubic centimeter ($10^{20}/cm^3$). In some applications, this doped material may present problems. One problem is an intrinsic tensile stress, which, when the boron-doped layer is relatively thick, can produce severe wafer bow. This wafer bow is incompatible with some fabrication steps. Another problem is that the thickness of the epitaxial layer may be limited due to technological reasons, for example, deposition conditions. Yet another problem is that the Young modulus of the boron-doped material may be lower than that of silicon, and may not be well known and understood.

In addition, the intrinsic losses of the boron-doped material may be higher than those of low-doped silicon. In the lost wafer process, the final release of the mechanical structure is often performed using a long, wet-etching step, which can be based on ethylene-diamine-pyrocathacol (EDP) solution, which requires careful control to maintain industrial hygiene standards during manufacture. What would be desirable is a fabrication process that eliminates the need for highly doped silicon and does not require a wet-etching step using EDP.

Summary of the Invention

The present invention includes methods for making thin silicon cantilevered or suspended structures which can be used to make Micro Electro Mechanical Systems (MEMS). The thin, silicon suspended structure can be used in a number of applications including, for example, accelerometers, gyroscopes, inertial sensing devices and so on. One illustrative embodiment of the present invention begins with a glass wafer and a silicon-on-insulator (SOI) wafer. The SOI wafer includes an insulator layer such as an oxide layer disposed between a first silicon layer and a second silicon layer. The insulator layer may be, for example, a silicon oxide layer.

In one illustrative embodiment, one or more recesses are formed in the glass wafer surface using standard photolithography and etching techniques. After formation of the recesses, electrodes may be formed at least partially within the recesses and, in some embodiments, on the surface of the glass wafer itself, if desired. The electrodes within the recesses may serve as, for example, one plate of a capacitor for sensing distance to, or vibration of, a later added suspended structure disposed over the recess.

The SOI wafer is bonded to the glass wafer, over the recessed and non-recessed portions, using an appropriate method such as anodic bonding, adhesives, heat bonding or any other suitable means. After bonding, the silicon layer of the SOI wafer that is located away from the glass wafer may be removed, using the insulator layer as an etch stop. The insulator layer can then be removed, leaving a single thin silicon layer. A photolithography and etching step can be used to pattern the remaining silicon layer in order to define the desired structure. Preferably, a DRIE process or other suitable process is used to pattern the remaining silicon layer. Suitable structures include tuning forks, combs, and cantilevered structures, among others.

In another illustrative embodiment of the present invention, a glass wafer or substrate, and an SOI wafer with a metal layer on one surface thereof are provided. Like above, and in one illustrative embodiment, the glass wafer may be etched to form a recess or recesses in the glass wafer surface, and electrodes may be formed on the glass wafer surface and/or in the recesses. At least a portion of the metal layer on

the SOI wafer is preferably patterned to coincide with the recesses in the glass wafer. The SOI wafer may then be bonded to the glass wafer surface, with the metal layer toward the glass wafer. After bonding, the silicon layer of the SOI wafer that is located away from the glass wafer may be removed, using the insulator layer as an etch stop. The insulator layer is then removed, leaving a single thin silicon layer bonded to the glass wafer.

A photolithographic and DRIE or other suitable process may then be used to etch the remaining silicon layer into a desired pattern, preferably in the region above the patterned metal layer. The etchant is preferably selected to etch through the remaining silicon layer but not through the underlying metal layer. The metal layer thus may act as an etch stop. The metal layer is believed to allow for sharper feature definition at the silicon-metalization layer interface, and also provides a barrier during the silicon etch step that may prevent gases in the recesses from escaping into the atmosphere, such as into a DRIE chamber. After etching of the remaining silicon layer, the metal layer may be removed using standard etching techniques.

Brief Description of the Drawings

Figure 1A is a highly diagrammatic, longitudinal, cross-sectional view of a glass wafer and a silicon-on-insulator wafer having a silicon oxide layer disposed between first and second silicon layers;

Figure 1B is a highly diagrammatic, longitudinal, cross-sectional view of the glass wafer of Figure 1A after recess formation;

Figure 1C is a highly diagrammatic, longitudinal, cross-sectional view of the glass wafer of Figure 1B, after electrode formation;

Figure 1D is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer of Figure 1A bonded to the glass wafer of Figure 1B;

Figure 1E is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 1D after removal of the second silicon layer;

Figure 1F is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 1D after removal of the silicon oxide layer;

Figure 1G is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 1F after selective etching through the first silicon layer;

Figure 2A is a highly diagrammatic, longitudinal, cross-sectional view of a glass wafer and a silicon-on-insulator wafer having a silicon oxide layer disposed between first and second silicon layers, where the first silicon layer surface is partially coated with a metal layer;

Figure 2B is a highly diagrammatic, longitudinal, cross-sectional view of the glass wafer of Figure 2A after recess formation;

Figure 2C is a highly diagrammatic, longitudinal, cross-sectional view of the glass wafer of Figure 2B after electrode formation;

Figure 2D is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer of Figure 2A bonded to the glass wafer of Figure 2B;

Figure 2E is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 2D after removal of the second silicon layer;

Figure 2F is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 2E after removal of the silicon oxide layer;

Figure 2G is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 2F after selective etching through the first silicon layer;

Figure 2H is a highly diagrammatic, longitudinal, cross-sectional view of the silicon-on-insulator wafer and glass wafer of Figure 2G after removal of the metal layer;

Figures 3A-3C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 1A-1D above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer; and

Figures 4A-4C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 2A-2D above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer.

Detailed Description of the Invention

Figure 1A illustrates a silicon-on-insulator (SOI) wafer 21 having a first silicon wafer or layer 20, an insulator wafer or layer 50, and a second silicon wafer or layer 60. First silicon layer 20 has a first surface 28, and a second substantially co-planar surface 26 abutting insulator layer 50. In one embodiment, insulator layer 50 is an oxide layer, such as silicon oxide. The first silicon layer 20 is preferably undoped or substantially undoped (such as less than $10^{18}/cm^3$, and more preferably less than about $10^{17}/cm^3$, and has a thickness of about between 5 and 200 microns or more preferably between about 10 and 100 microns, depending on the application. A glass wafer or substrate 22 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 22 has a first surface 24 and substantially co-planar second surface 25.

To form an accelerometer, tuning fork, or gyroscope or the like, recesses may be formed in the top surface 24 of the glass wafer. In Figure 1B, a first recess 30 and a second recess 34 are etched into the top surface 24 of the glass wafer 22. The first recess has a first recessed surface 32 and the second recess 34 has a second recessed surface 36. In some embodiments of the present invention, the recesses are used to form a capacitive gap for the detection of displacement of inertial electrodes, and are formed using standard etching techniques well known to those skilled in the art.

Figure 1C illustrates glass wafer 22 after electrodes 38 and 40 have been formed on the first recessed surface 32 and the second recessed surface 36. Although electrodes 38 and 40 are shown covering substantially all of the recesses surfaces 32 and 36, it is contemplated that only a portion of the recessed surfaces 32 and 36 may be covered, if desired. In addition, the second recess 34 has an electrode tab or ear 42 extending nearer the unrecessed surface of the glass wafer 22. This may or may not be required, depending on the application. Metal electrodes 38 and 40 are preferably formed using techniques well known to those skilled in the art. In one illustrative embodiment, the electrodes are titanium-platinum or gold-based electrodes.

Figure 1D illustrates SOI wafer 21 and glass wafer 22 after the first surface 28 of the first silicon layer 20 of SOI wafer 21 has been bonded to glass wafer 22. As may be seen from inspection of Figure 1D, SOI wafer 21 has been bonded over both

recessed and nonrecessed portions of glass wafer 22. In one embodiment, SOI wafer 21 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding, etc.

Figure 1E illustrates the removal of the second silicon layer 60 from SOI wafer 21. In one embodiment, second silicon layer 60 is removed through etching. In a preferred embodiment, silicon layer 60 is thinned down by grinding or KOH etching, followed by final etching using a Reactive Ion Etch (RIE) down to oxide layer 50. Next, the oxide layer may be removed. Figure 1F shows the structure after the oxide layer 50 has been removed, preferably using a Buffered Oxide Etch Solution (BOE) etching process.

Figure 1G illustrates the first silicon layer 20 of SOI wafer 21 after an etch has been performed on second surface 26 of first silicon layer 20. When forming a typical device, such as an accelerometer, tuning fork, or gyroscope, several etched regions 44 may be formed. Preferably, the silicon etch extends through the first silicon layer 20 and into recesses 30 and 34 of the glass wafer 22. The silicon is preferably etched using standard silicon etching procedures, such as a Deep Reactive Ion Etch (DRIE) process. Preferably, a standard photolithography process is used to define the desired structural shapes in the silicon wafer 20. Examples of suitable shapes include, but are not limited to, cantilevered beams, suspended beams, combs, tuning forks, plates, etc.

In another illustrative embodiment, and referring now to Figure 2A, a SOI wafer 121 is provided. Like above, the SOI wafer 121 has a first silicon layer 120, an oxide layer 50, and a second silicon layer 60. A metal layer 129 is then provided on a first surface of the first silicon layer 120 of the SOI wafer. The metal layer 129 may be provided as part of the originally supplied SOI wafer 121, or may be deposited or otherwise formed thereupon using conventional methods. One suitable metal for the formation of metal layer 129 is chromium on oxide, although other metals or alloys may be used.

Figure 2B illustrates a glass wafer 22 after recesses 30 and 34 have been formed, as previously discussed above with respect to Figure 1B above. Figure 2C illustrates glass wafer 22 after formation of electrodes 38 and 40, as previously discussed with respect to Figure 1C. Preferably, the metal layer 129 is patterned so

that the remaining metal corresponds to or is otherwise defined to fit within recesses 30 and 34.

In Figure 2D, the metalized SOI wafer 121 is shown bonded to the glass wafer 22, with the metal layer 129 situated adjacent the glass wafer 22. One method for bonding the SOI wafer 121 to the glass wafer 22 is anodic bonding. A by-product of some anodic bonding processes is the release of oxygen. As can be seen, the cavities formed between the recesses 30 and 34 and the SOI wafer 121 may collect the oxygen released during the anodic bonding process, and thus may have an increased concentration thereof.

Figure 2E shows the structure after the second silicon layer 60 of the SOI wafer 121 is removed. In a preferred embodiment, silicon layer 60 is thinned by grinding or KOH etching, followed by a final etch down to the oxide layer 50 using a Reactive Ion Etch (RIE). Figure 2F illustrates the structure after the oxide layer 50 of the SOI wafer 121 has been removed. In one embodiment, oxide layer 50 is removed through stripping in a BOE etching process.

Figure 2G shows the remaining first silicon layer 120 after a pattern has been etched therein to form the desired structure. The etching preferably includes a suitably selective etchant that etches through the first silicon layer 120, but not through metal layer 129. Standard lithography techniques can be used to form the series of recesses, channels, or holes 144 through the silicon wafer 120, but not through the metal layer 129. The metal layer 129 thus may serve as an etch stop layer. It has been found that by providing an etch stop layer, sharper feature definition at the interface of the silicon wafer 120 and the metal layer 129 can be achieved, resulting in more precise feature definition in the resulting silicon structure.

Another benefit of providing metal layer 129 is that a seal or barrier is provided to prevent gasses from escaping from recesses 30 and 34 into the atmosphere during the silicon etching process. This can be particularly important when the remaining silicon layer 120 is etched using an etching process that relies at least in part on the gas composition in the surrounding atmosphere, such as a DRIE etching process. The release of gases, such as oxygen which as described above may be collected in the recesses 30 and 34 during the anodic bonding process, can effect

the effectiveness and/or controllability of some etching processes, such as a DRIE etching process.

Figure 2H illustrates the remaining silicon layer 120 and glass wafer 22 after the metal layer 129 has been removed. The metal layer 129 may be removed in recess areas 30 and 34 using techniques well known to those skilled in the art. In one example, an etchant capable of removing the metal layer 129, but not the silicon wafer 120, may be applied to the silicon wafer recesses 144. The etchant may thus dissolve metal layer 129. In a preferred embodiment, the etchant is capable of removing metal layer 129, but does not remove electrodes 38 and 40.

Figures 3A-3C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 1A-1D above, but with the recess or recesses formed in the silicon wafer 150 rather than the glass wafer 182. Figure 3A illustrates a silicon-on-insulator (SOI) wafer 150 having a first silicon wafer or layer 160, an insulator wafer or layer 154, and a second silicon wafer or layer 152. First silicon layer 160 has a first surface 162. A first recess 170 and a second recess 172 are etched into the first surface 162 of the first silicon wafer or layer 160, as shown. Preferably, the first recess 170 and the second recess 172 do not extend all the way through the first silicon wafer or layer 160. The first recess 170 has a first recessed surface 174 and the second recess 172 has a second recessed surface 176. In some embodiments, the recesses are used to form a capacitive gap for the detection of displacement of inertial electrodes, and are formed using standard etching techniques well known to those skilled in the art. A glass wafer or substrate 182 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 182 has a first surface 184.

Figure 3B illustrates the glass wafer 182 after electrodes 190 and 192 have been formed on the first surface 184 of the glass wafer 182. Figure 3C also illustrates SOI wafer 150 and glass wafer 182 after the first surface 162 of the first silicon layer 160 of SOI wafer 150 has been bonded to the first surface 184 of glass wafer 182. In one embodiment, SOI wafer 150 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding,

etc. The remaining processing steps may be similar to that shown and described above with respect to Figures 1E-1G.

Figures 4A-4C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 2A-2D above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer. Like in Figure 2A, an SOI wafer 200 has a first silicon layer 202, an oxide layer 204, and a second silicon layer 206. First silicon layer 202 has a first surface 210. A first recess 212 and a second recess 214 are etched or otherwise formed into the first surface 210 of the first silicon wafer or layer 202, as shown. Preferably, the first recess 212 and the second recess 214 do not extend all the way through the first silicon wafer or layer 202. The first recess 212 has a first recessed surface 216 and the second recess 214 has a second recessed surface 218. A glass wafer or substrate 220 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 220 has a first surface 222.

As shown in Figure 4B, a metal layer 226 is provided on the first recessed surface 216 and the second recessed surface 218 of the SOI wafer 200. The metal layer is preferably deposited or otherwise formed thereupon using conventional methods. One suitable metal for the formation of metal layer 226 is chromium on oxide, although other metals or alloys may be used. Figure 4B also illustrates the glass wafer 220 after electrodes 230 and 232 have been formed.

Figure 4C shows SOI wafer 200 and glass wafer 220 after the first surface 210 of the first silicon layer 202 of SOI wafer 200 has been bonded to the glass wafer 220. In one embodiment, SOI wafer 200 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding, etc. The remaining processing steps may be similar to that shown and described above with respect to Figures 2E-2H.

While the above illustrative embodiments use an SOI wafer and a glass wafer, it is contemplated that any other suitable material systems may be used. For example, rather than using a silicon-on-insulator (SOI) wafer having a first silicon wafer or layer, an insulator wafer or layer, and a second silicon wafer or layer, it is

second layer may be used. Likewise, rather than using a glass wafer, any fairly rigid substrate may be used.

Numerous advantages of the invention covered by this document have been set forth in the foregoing description. It will be understood, however, that this disclosure is, in many respects, only illustrative. Changes may be made in details, particularly in matters of shape, size, and arrangement of parts without exceeding the scope of the invention. For example, while the above illustrative embodiments include a silicon-on-insulator wafer bonded to a glass wafer or substrate, other material systems may be used. The invention's scope is, of course, defined in the language in which the appended claims are expressed.

1. A method for making a thin silicon suspended structure characterized by:

providing a glass wafer (22) or substrate having a surface (24);

providing an SOI wafer (21) having an insulating layer (50) disposed between a first silicon layer (20) and a second silicon layer (60);

forming a recess (30) in said glass wafer surface (24) or said first silicon layer (20) of said SIO wafer (21);

bonding said SOI wafer (21) to said glass wafer surface (24) such that at least part of said first silicon layer (20) is bonded to said glass wafer surface (24) so that at least part of said first silicon layer (20) overhangs said recess (30);

removing said second silicon layer (60) of the SOI wafer (21);

removing the insulating layer (50) of the SOI wafer (21); and

selectively patterning the first silicon layer (20) of the SOI wafer (21) to form a thin silicon suspended structure that at least partially overhangs said recess (30).

2. A method for making a thin silicon suspended structure as in claim 1, further characterized by forming at least one electrode (38) on said glass wafer surface (24) that is in alignment with at least part of said recess (30).

3. A method for making a thin silicon suspended structure as in claim 1, wherein said bonding step includes anodic bonding.

4. A method for making a thin silicon suspended structure characterized by:

providing a glass wafer (22) or substrate having a surface (24);

providing a SOI wafer (121) having an insulating layer (50) disposed between a first silicon layer (120) and a second silicon layer (60);

forming a recess (30) in said glass wafer surface (24) or the first silicon layer (120) of the SOI wafer (21);

providing a patterned metal layer (129) adjacent the first silicon layer (120), the patterned metal layer (129) coinciding with at least part of said recess (30);

bonding said SOI wafer (121) to said glass wafer surface (24) such that at least part of said first silicon layer (120) is bonded to said glass wafer surface (24) so that at least part of said first silicon layer (120) overhangs said recess (30);

removing said second silicon layer (60);

removing said insulating layer (50);

selectively patterning the first silicon layer (120) to form a thin silicon suspended structure that at least partially overhangs said recess (30); and

removing said metal layer (129).

5. A method for making a thin silicon suspended structure as in claim 4, wherein said bonding step includes anodic bonding.

6. A method for making a thin suspended structure characterized by:

providing a first wafer (22) or substrate having a surface (24);

providing a second wafer (121) having an etch stop layer (50) disposed between a first layer (120) and a second layer (60);

forming a recess in said first wafer surface (30) or in said second wafer;

bonding said second wafer (121) to said first wafer surface (24) such that at least part of said first layer (120) of said second wafer (121) is bonded to said first wafer surface (24) so that at least part of said first layer (120) overhangs said recess (24);

removing said second layer (60) of the second wafer (121);

removing the etch stop layer (50) of the second wafer (121); and

selectively patterning the first layer (120) of the second wafer (121) to form a thin suspended structure that at least partially overhangs said recess (30).

FIG. 1A

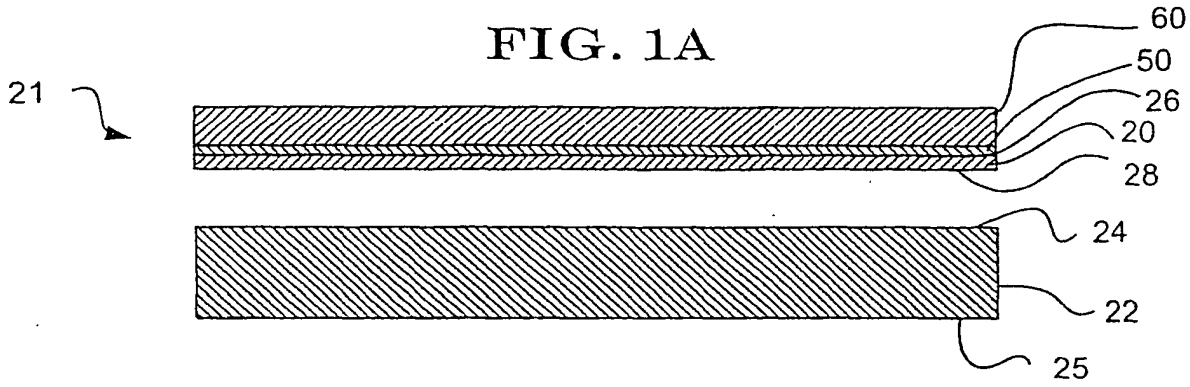


FIG. 1B

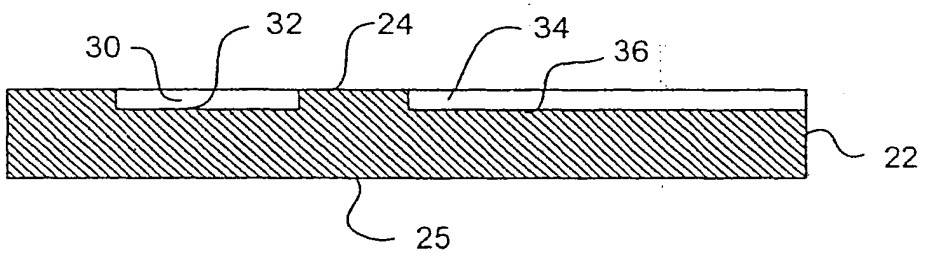


FIG. 1C

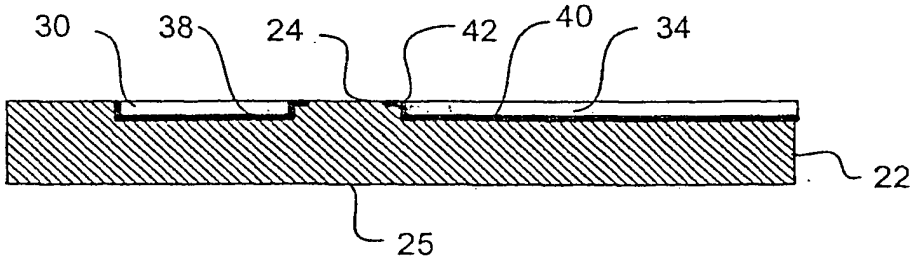


FIG. 1D

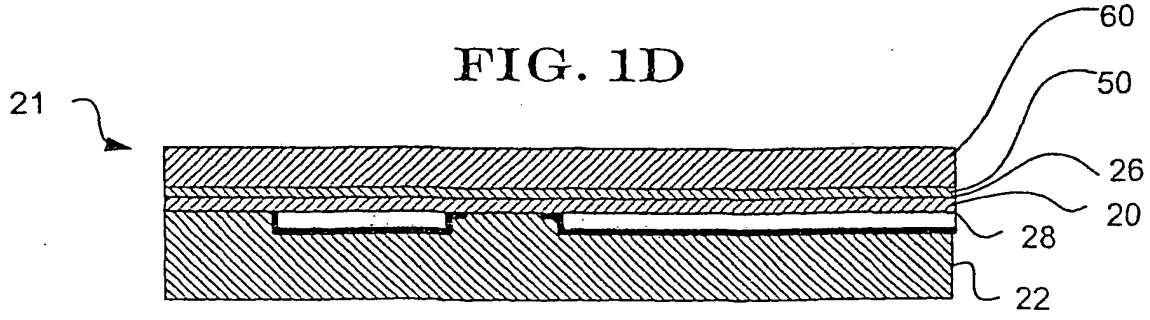


FIG. 1E

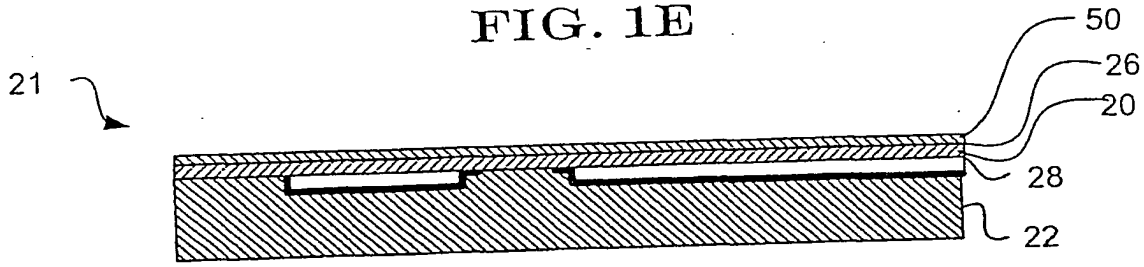


FIG. 1F

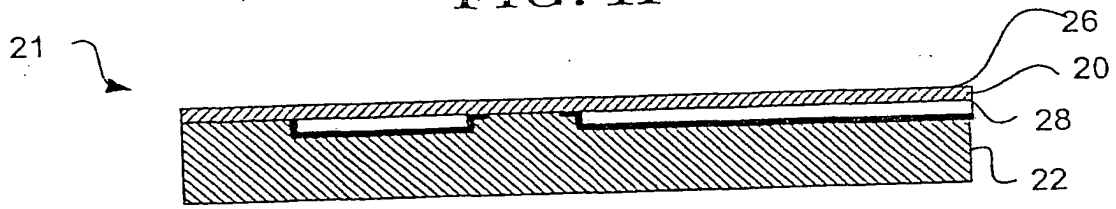


FIG. 1G

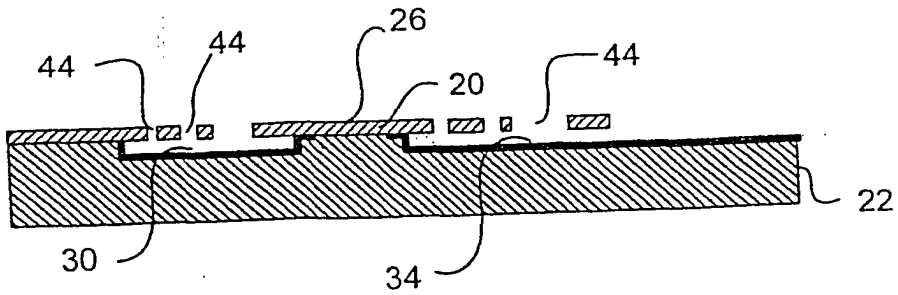


FIG. 2A

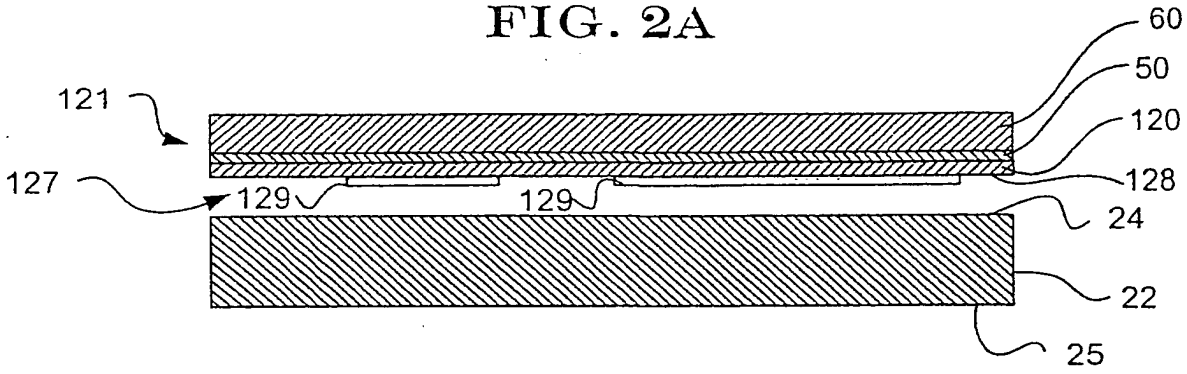


FIG. 2B

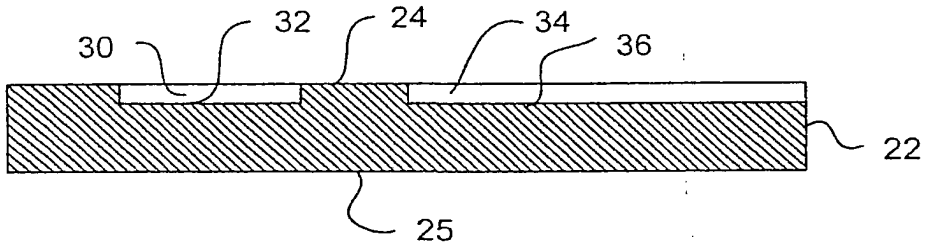


FIG. 2C

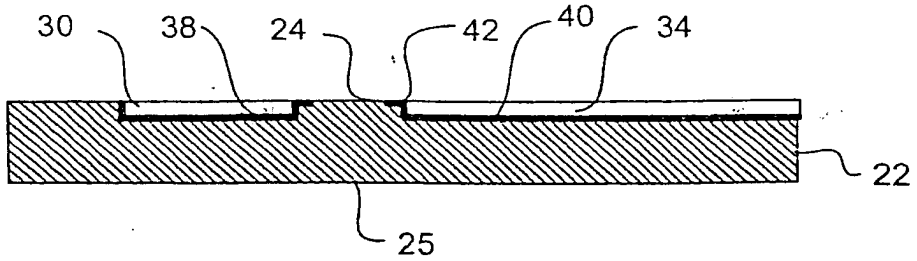


FIG. 2D

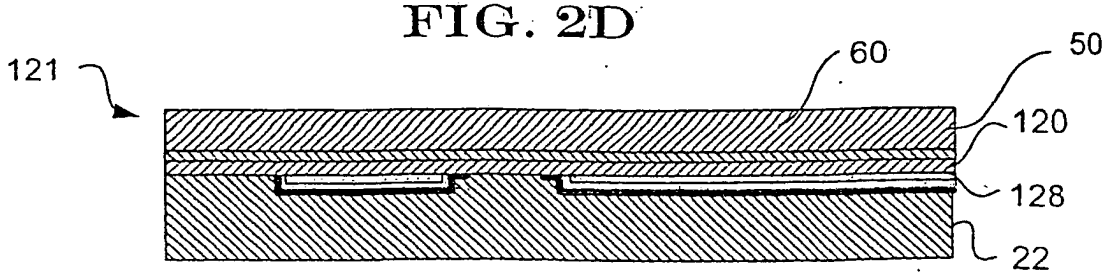


FIG. 2E

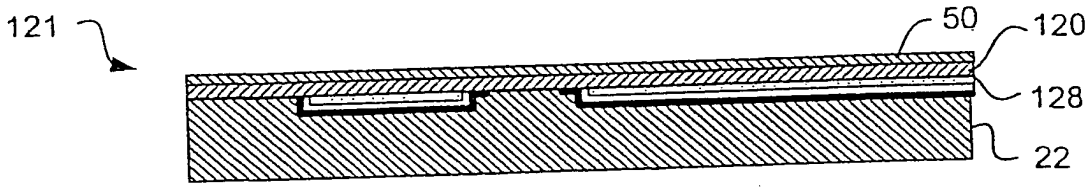


FIG. 2F

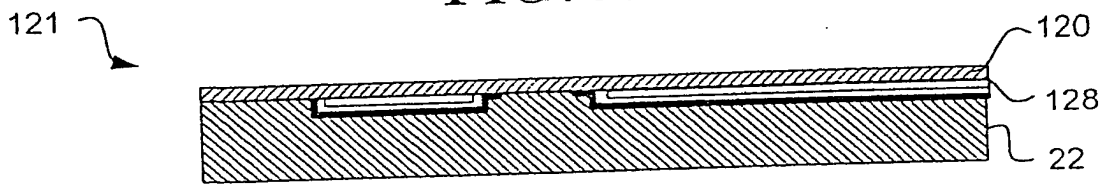


FIG. 2G

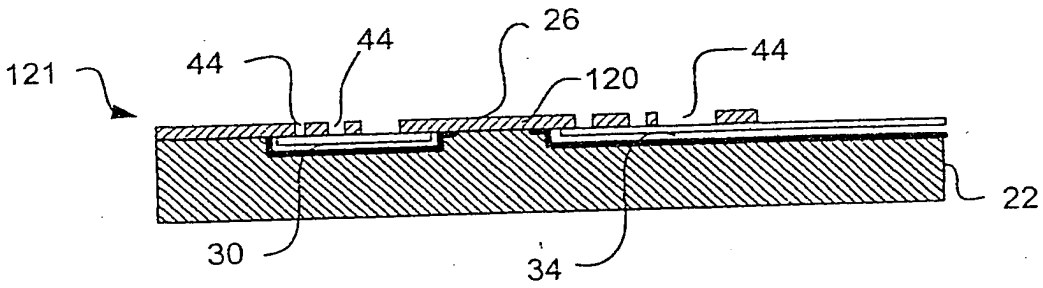


FIG. 2H

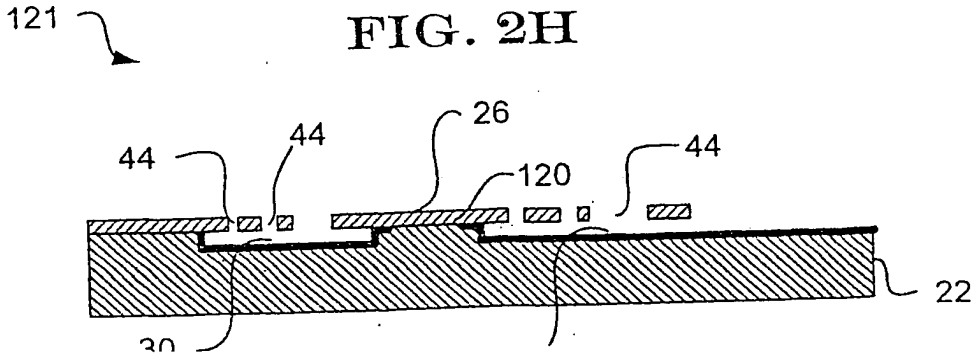


FIG. 3A

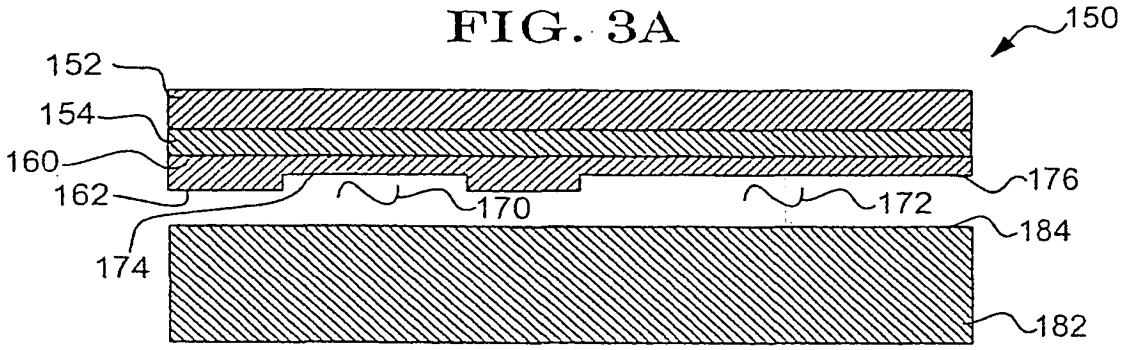


FIG. 3B

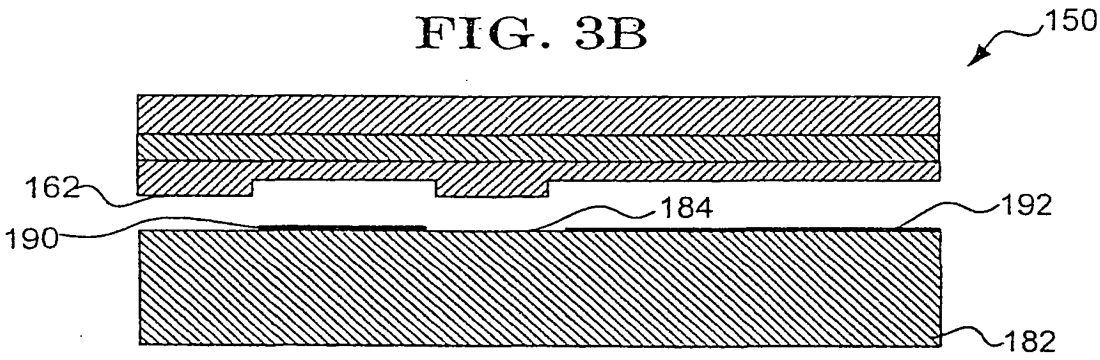


FIG. 3C

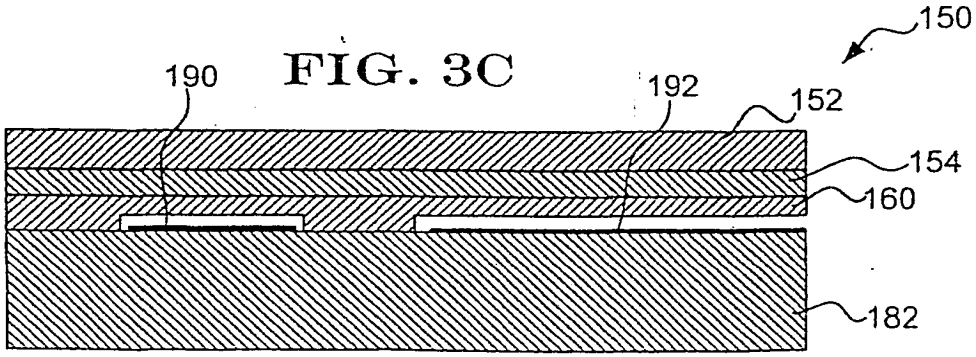


FIG. 4A

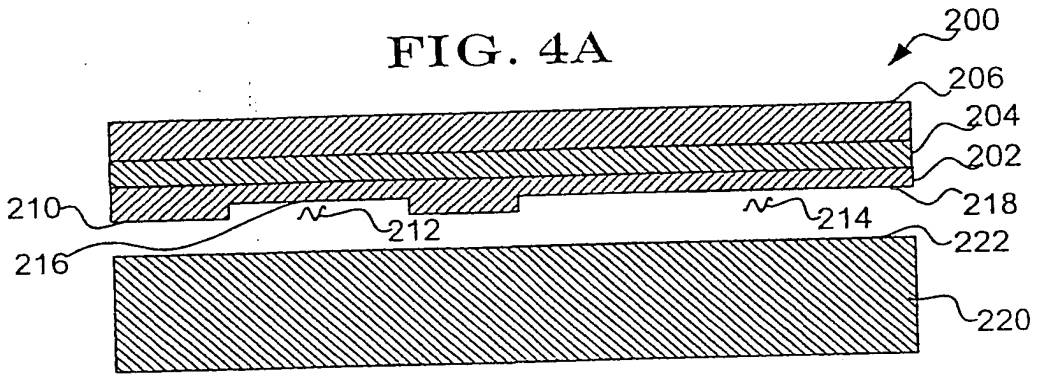


FIG. 4B

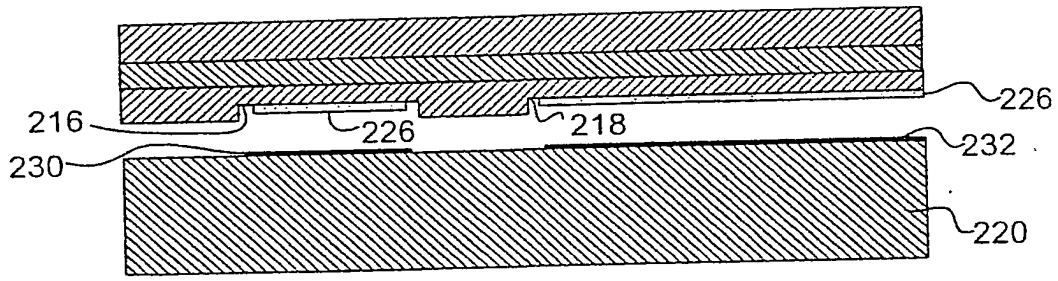
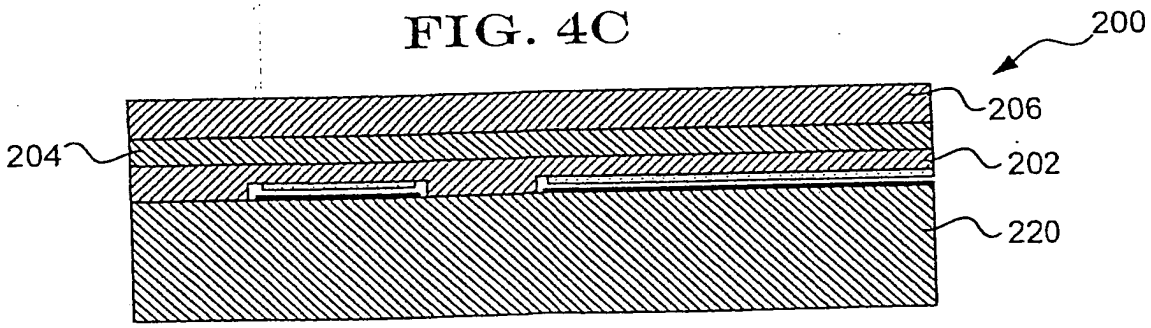


FIG. 4C



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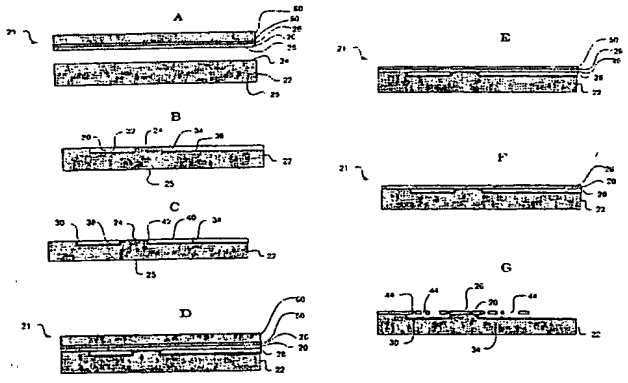
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOI/GLASS PROCESS FOR FORMING THIN SILICON MICROMACHINED STRUCTURES



(57) Abstract: Methods for making thin silicon layers suspended over recesses (30) in glass wafers (22). One method includes providing a thin silicon-on-insulator (SOI) wafer (21), and a glass wafer (22). The SOI wafer (21) can include a silicon oxide layer (50) disposed between a first undoped or substantially undoped silicon layer (20) and a second silicon layer (60). Recesses (30) can be formed in the glass wafer surface (24) and electrodes (38) may be formed on the glass wafer surface (24). The first silicon layer (20) of the SOI wafer (21) is then bonded to the glass wafer surface (24) having the recesses (30), and the second silicon layer (60) is subsequently removed using the silicon oxide layer (50) as an etch stop. Next, the silicon oxide layer (50) is removed. The first silicon layer (20) can then be etched to form the desired structure. In another illustrative embodiment, the first silicon layer (120) has a patterned metal layer (129) positioned adjacent the recesses (30) in the glass wafer (22). The, the second silicon layer (60) is

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INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 B81C1/00 B81B3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B81C B81B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, IBM-TDB, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MOCHIDA Y ET AL: "A micromachined vibrating rate gyroscope with independent beams for the drive and detection modes" SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 80, no. 2, March 2000 (2000-03), pages 170-178, XP004192104 ISSN: 0924-4247 * Section 4 Fabrication * figure 7 ---	1-6
P,X	WO 00 78667 A (HONEYWELL INC) 28 December 2000 (2000-12-28) figures 1,2 --- -/--	1,6

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 November 2002	06/12/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	McGinley, C

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/50089

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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A	US 4 855 544 A (GLENN MAX C) 8 August 1989 (1989-08-08) column 1, line 59 -column 2, line 19 ---	1-6
A	US 5 343 064 A (SPANGLER LELAND J ET AL) 30 August 1994 (1994-08-30) column 10, line 4 - line 45; figures 8,9 -----	1-6

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		EP 1187789 A1	20-03-2002
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